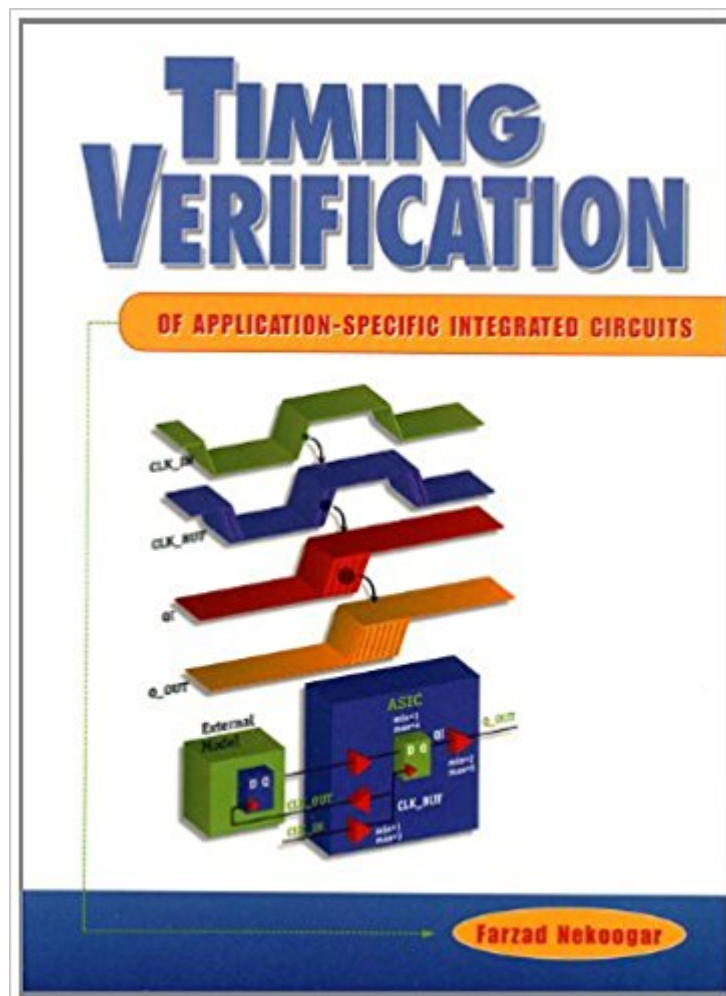


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Timing Verification Of Application-Specific Integrated Circuits (ASICs)



Synopsis

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Book Information

Paperback: 208 pages

Publisher: Prentice Hall; 1 edition (June 24, 1999)

Language: English

ISBN-10: 0137943482

ISBN-13: 978-0137943487

Product Dimensions: 7 x 0.7 x 9 inches

Shipping Weight: 12 ounces

Average Customer Review: 4.6 out of 5 starsÂ Â See all reviewsÂ (5 customer reviews)

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Customer Reviews

The book has detailed information on timing issues of ASICs and FPGAs, such as pre and post layout timing analysis. Several comprehensive examples on timing analysis using different available STA tools makes the book a practical guide for verification engineers. The book also covers some RTL coding examples for timing, however it is made solely for timing verification not a book for learning HDL languages, therefore trying to criticize the programming part of the book as in previous review is irrelevant let alone trying to correct spelling.

This is a really good book for the beginners to understand the timing verification in ASIC flow. There are not many books in this area which explain things clearly. Most of them get lost in the syntax and modules of coding. 90% percent of ASIC design is done with synopsys tools and book authors tell more about the tool syntax than why they are there. This book has minimum of tool syntax. It is SIMPLE and that is its greatest quality. Most people who have reviewed the book have given good ratings. The one that is bad must be from an experienced person. This book is not for an expert in this field.

This book is very good for beginners starting working with FPGAs. Probably ASIC designers need some more, I don't know I am not one of them. Timing analysis is a topic which is unfortunately not very well known by lots of engineers working on small/medium size FPGA projects. For them, I would recommend to buy/read this book. It was written 10 years ago for ASICs and now it is still good for FPGAs for learning how to setup simple timing constraints on smaller FPGAs, (for example a PCI, IDE or LPC bus interfaces on a 100kgate Xilinx Spartan-III FPGA) or how to design our logic for higher speed. I knew some things about timing analysis already, so this book taught me a little more. Now I have purchased the "Static Timing Analysis for Nanometer Designs", which is much thicker and more detailed, so I hope I will learn a lot more from that one. Although these books say ASIC and nanometer-design in their titles, they provide valuable information also for design engineers working with FPGAs, CPLDs or board-level designs.

A clearly written, concise, and very helpful book.

Not a bad book for general introductory info on timing, but very little advanced detail for the experienced designer. There are a few errors in the Verilog examples. No big deal because little of the book is language specific. Good concepts presented but don't blindly follow any of the suggestions without really understanding them. Example 3.2 This module will not compile. - the sensitivity list is written like VHDL - he uses 'define statements then forgets to use a backtick when the definition is used Example 3.7 - Keyword is 'endmodule' not 'end module'

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